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Reg. No. : .....

Name : .....

Fourth Semester B.Tech. Degree Examination, June 2016
(2013 Scheme)
13.402 : DIGITAL ELECTRONICS AND LOGIC DESIGN (E)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions : **(10×2=20 Marks)**

1. Realize an XOR gate using NOR gates.
2. i) Convert $(378.93)_{10}$ to octal.
   ii) Convert $(756.603)_8$ to hexa decimal.
3. What is fan in and fan out ?
4. Realize a circuit which can generate parity bit for the given four bit data.
5. Compare a multiplexer and demultiplexer.
6. How will you convert RS flip-flop into JK flip-flop ?
7. What is the difference between level triggering and edge triggering ?
8. What is race around problem ?
9. Explain EPROM.
10. What are the basic classifications of RAM ?

PART – B

Answer **any one** question from **each** Module :

Module – I

11. a) Reduce the expression using K map and implement the function using NAND gate $\sum m = (0, 1, 4, 5, 6, 7, 9, 11, 15) + d\ (10, 14)$. **10**
    b) What are universal gates ? Why are they called universal ? **5**
    c) What is gray code ? Find the binary equivalent of the gray code (1110). **5**

OR

12. a) Simplify the expression using Quine Mc Clusky method.

$F(w, x, y, z) = \sum m(0, 1, 2, 8, 10, 11, 14, 15)$ 12

b) Simplify using Boolean algebra.

$F = w\bar{x} + \bar{y}\bar{z} + \bar{w}y\bar{z}$ and implement using universal gates. 8

Module – II

13. a) Design a 4 bit full adder with carry look ahead generator. 12

b) Use a multiplexer having three select input to implement the logic function $f = \sum m(0, 1, 4, 10, 11, 14, 15)$. 8

OR

14. a) With the help of relevant circuit schematics, briefly describe the operation of CMOS NAND and NOR gates. 10

b) What are the classifications of logic family ? Compare their characteristics. 10

Module – III

15. a) Design and implement a 3 bit synchronous up/down counter using JK flip-flop. 12

b) With circuit diagram explain 4 bit PIPO shift register. 8

OR

16. a) Explain the operational basics of binary ripple counters. Implement a 3 bit binary ripple counter using JK flip-flop. 10

b) Explain 4 bit Johnson counter with waveforms. 10

Module – IV

17. a) Design astable and monostable multivibrators using discrete gates. Explain its working. 12

b) What is the difference between static and dynamic RAM ? 8

OR

18. a) Give the advantages of programmable logic devices over fixed logic devices. Explain PAL architecture. 14

b) Differentiate between ROM and RAM. 6